WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Monday, June 28, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
☐	L16	reconfigur$4 with (data path) with (instruction$1 or command$1)	34
		DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ	
☐	L15	reconfigur$4 with data path	25
☐	L14	data flow instruction$1	10
☐	L13	instruction$1 and L11	6
☐	L12	instruction$1 with L11	0
☐	L11	reconfigur$4 with (i/o or input/output)	64
		DB=PGPB,USPT; PLUR=NO; OP=ADJ	
☐	L10	instruction$1 with L9	50
☐	L9	reconfigur$4 with (i/o or input/output)	704
☐	L8	programable i/o	5
☐	L7	L6 not l5	6
☐	L6	5970254.uref.	12
☐	L5	6282627.uref.	19
☐	L4	l1 and data path	2
☐	L3	configuration memory and l1	2
☐	L2	(instruction$1 with data path) and L1	0
☐	L1	wong.in. and (programmable data path).ti.	2

END OF SEARCH HISTORY

WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Monday, June 28, 2004

Hide?	Set Name	Query	Hit Count
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ		
☐	L14	data flow instruction$1	10
☐	L13	instruction$1 and L11	6
☐	L12	instruction$1 with L11	0
☐	L11	reconfigur$4 with (i/o or input/output)	64
	DB=PGPB,USPT; PLUR=NO; OP=ADJ		
☐	L10	instruction$1 with L9	50
☐	L9	reconfigur$4 with (i/o or input/output)	704
☐	L8	programable i/o	5
☐	L7	L6 not l5	6
☐	L6	5970254.uref.	12
☐	L5	6282627.uref.	19
☐	L4	l1 and data path	2
☐	L3	configuration memory and l1	2
☐	L2	(instruction$1 with data path) and L1	0
☐	L1	wong.in. and (programmable data path).ti.	2

END OF SEARCH HISTORY

Generate Collection | Print

L3: Entry 1 of 2 File: USPT Aug 28, 2001

US-PAT-NO: 6282627
DOCUMENT-IDENTIFIER: US 6282627 B1

TITLE: Integrated processor and programmable data path chip for reconfigurable computing

DATE-ISSUED: August 28, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wong; Dale	San Francisco	CA		
Phillips; Christopher E.	San Jose	CA		
Cooke; Laurence H.	Los Gatos	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Chameleon Systems, Inc.	Sunnyvale	CA			02

APPL-NO: 09/ 446762 [PALM]
DATE FILED: May 25, 2000

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102(E)-DATE
PCT/US98/13565	June 29, 1998	WO99/00739	Jan 7, 1999	May 25, 2000	May 25, 2000

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 712/15; 712/13
US-CL-CURRENT: 712/15; 712/13

FIELD-OF-SEARCH: 712/37, 712/11, 712/13, 712/15, 712/20

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5500609	March 1996	Kean	326/41
☐	5535342	July 1996	Taylor	395/307
☐	5535406	July 1996	Kolchinsky	395/800
☐	5552722	September 1996	Kean	326/41
☐	5583749	December 1996	Tredennick et al.	361/790
☐	5603043	February 1997	Taylor et al.	395/800

☐	5613146	March 1997	Gove et al.	395/800
☐	5617577	April 1997	Barker et al.	395/800
☐	5652875	July 1997	Taylor	395/500
☐	5680634	October 1997	Estes	395/804
☐	5748979	May 1998	Trimberger	395/800.37
☐	5752006	May 1998	Baxter	395/500
☐	5956518	September 1999	Delton	712/15
☐	5963745	October 1999	Collins	712/13
☐	6023742	February 2000	Ebeling	710/107

ART-UNIT: 273

PRIMARY-EXAMINER: Coleman; Eric

ATTY-AGENT-FIRM: Burns Doane Swecker & Mathis

ABSTRACT:

The present invention, generally speaking, provides a reconfigurable computing solution that offers the flexibility of software development and the performance of dedicated hardware solutions. A reconfigurable processor chip includes a standard processor, blocks of reconfigurable logic (1101, 1103), and interfaces (319a, 319b, 311) between these elements. The chip allows application code to be recompiled into a combination of software and reloadable hardware blocks using corresponding software tools. A mixture of arithmetic cells and logic cells allows for higher effective utilization of silicon than a standard interconnect. More efficient use of configuration stack memory results, since different sections of converted code require different portions of ALU functions and bus interconnect. Many types of interfaces with the embedded processor are provided, allowing for fast interface between standard processor code and configurable "hard-wired" functions.

29 Claims, 30 Drawing figures

First Hit Fwd Refs

Generate Collection Print

L5: Entry 10 of 19 File: USPT Nov 11, 2003

US-PAT-NO: 6647511
DOCUMENT-IDENTIFIER: US 6647511 B1

TITLE: Reconfigurable datapath for processor debug functions

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		
Karthikeyan; Madathil R.	Bangalore			IN
Menon; Amitabh	Bangalore			IN
Matt; David R.	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 09/ 379769 [PALM]
DATE FILED: August 24, 1999

PARENT-CASE:
This application claims the benefit of provisional application No. 60/100,712, filed Sep. 17,1998.

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/30; 714/733, 714/734
US-CL-CURRENT: 714/30; 714/733, 714/734

FIELD-OF-SEARCH: 714/723, 714/733, 714/734, 714/30, 714/27, 714/40

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5338984	August 1994	Sutherland	326/41
☐	5974435	October 1999	Abbott	708/523
☐	6058469	May 2000	Baxter	712/43
☐	6282627	August 2001	Wong et al.	712/15
☐	6510530	January 2003	Wu et al.	714/30

ART-UNIT: 2184

PRIMARY-EXAMINER: Beausoliel; Robert

ASSISTANT-EXAMINER: Duncan; Marc

ATTY-AGENT-FIRM: Petersen; Bret J. Brady, III; W. James Telecky, Jr.; Frederick J.

ABSTRACT:

A reconfigurable datapath (13b), which may be alternatively configured for various debug modes. These modes include a breakpoint mode (20), counter mode (30a-30c), DMA mode (40), and PSA mode (50). Each configuration uses one or more of two bitcell units: a register bitcell unit (60) and a comparator bitcell unit (70). The inputs and interconnections of these bitcell units (60, 70) determine the configuration, and hence the mode, for which they are to be used.

32 Claims, 9 Drawing figures

L5: Entry 10 of 19 File: USPT Nov 11, 2003

US-PAT-NO: 6647511
DOCUMENT-IDENTIFIER: US 6647511 B1

TITLE: Reconfigurable datapath for processor debug functions

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		
Karthikeyan; Madathil R.	Bangalore			IN
Menon; Amitabh	Bangalore			IN
Matt; David R.	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 09/ 379769 [PALM]
DATE FILED: August 24, 1999

PARENT-CASE:
This application claims the benefit of provisional application No. 60/100,712, filed Sep. 17,1998.

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/30; 714/733, 714/734
US-CL-CURRENT: 714/30; 714/733, 714/734

FIELD-OF-SEARCH: 714/723, 714/733, 714/734, 714/30, 714/27, 714/40

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5338984	August 1994	Sutherland	326/41
☐	5974435	October 1999	Abbott	708/523
☐	6058469	May 2000	Baxter	712/43
☐	6282627	August 2001	Wong et al.	712/15
☐	6510530	January 2003	Wu et al.	714/30

Full - [FULL]
Title - [TI]
Citation - [CIT]
Front - [FRO]
Review - [REV]
Classification - [C
Date - [DATE]
Reference - [REF]
Sequences - [SEQ
Attachments - [A
Claims - [CLM]
KWIC - [KWIC]
Drwg Desc - [DRA
Image - [IMG]

ART-UNIT: 2184

PRIMARY-EXAMINER: Beausoliel; Robert

ASSISTANT-EXAMINER: Duncan; Marc

ATTY-AGENT-FIRM: Petersen; Bret J. Brady, III; W. James Telecky, Jr.; Frederick J.

ABSTRACT:

A reconfigurable datapath (13b), which may be alternatively configured for various debug modes. These modes include a breakpoint mode (20), counter mode (30a-30c), DMA mode (40), and PSA mode (50). Each configuration uses one or more of two bitcell units: a register bitcell unit (60) and a comparator bitcell unit (70). The inputs and interconnections of these bitcell units (60, 70) determine the configuration, and hence the mode, for which they are to be used.

32 Claims, 9 Drawing figures

☐ Generate Collection | Print

L5: Entry 17 of 19 File: USPT Nov 5, 2002

US-PAT-NO: 6477643
DOCUMENT-IDENTIFIER: US 6477643 B1
**** See image for Certificate of Correction ****

TITLE: Process for automatic dynamic reloading of data flow processors (dfps) and units with two-or-three-dimensional programmable cell architectures (fpgas, dpgas, and the like)

DATE-ISSUED: November 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Vorbach; Martin	Karlsruhe			DE
Munch; Robert	Karlsruhe			DE

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
PACT GmbH	Munich			DE	03

APPL-NO: 09/ 613217 [PALM]
DATE FILED: July 10, 2000

PARENT-CASE:
This application is continuation of application Ser. No. 08/947,002 filed Oct. 8, 1997 now U.S. pat. No. 6,088,795.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
DE	196 54 846	December 27, 1996

INT-CL: [07] G06 F 9/00

US-CL-ISSUED: 713/100; 710/131, 712/15, 712/223, 713/1
US-CL-CURRENT: 713/100; 710/306, 712/15, 712/223, 713/1

FIELD-OF-SEARCH: 713/100, 713/1, 713/2, 712/220, 712/223, 712/16, 712/10, 712/15, 307/465, 709/221, 709/222, 714/3, 714/7, 395/500, 710/131

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4706216	November 1987	Carter	
☐	4739474	April 1988	Holsztynski et al.	

☐	4761755	August 1988	Ardini et al.
☐	4811214	March 1989	Nosenchuck et al.
☐	4870302	September 1989	Freeman
☐	4901268	February 1990	Judd
☐	4967340	October 1990	Dawes
☐	5014193	May 1991	Garner et al.
☐	5015884	May 1991	Agrawal et al.
☐	5021947	June 1991	Campbell et al.
☐	5023775	June 1991	Poret
☐	5081375	January 1992	Pickett et al.
☐	5109503	April 1992	Cruickshank et al.
☐	5123109	June 1992	Hillis
☐	5125801	June 1992	Nabity et al.
☐	5128559	July 1992	Steele
☐	5142469	August 1992	Weisenborn
☐	5204935	April 1993	Mihara et al.
☐	5208491	May 1993	Ebeling et al.
☐	5226122	July 1993	Thayer et al.
☐	RE34363	August 1993	Freeman
☐	5233539	August 1993	Agrawal et al.
☐	5247689	September 1993	Ewert
☐	5287472	February 1994	Horst
☐	5301284	April 1994	Estes et al.
☐	5301344	April 1994	Kolchinsky
☐	5303172	April 1994	Magar et al.
☐	5336950	August 1994	Popli et al.
☐	5347639	September 1994	Rechtschaffen et al.
☐	5361373	November 1994	Gilson
☐	5410723	April 1995	Schmidt et al.
☐	5418952	May 1995	Morley et al.
☐	5421019	May 1995	Holsztynski et al.
☐	5422823	June 1995	Agrawal et al.
☐	5426378	June 1995	Ong
☐	5430687	July 1995	Hung et al.
☐	5440245	August 1995	Galbraith et al.
☐	5440538	August 1995	Olsen et al.
☐	5442790	August 1995	Nosenchuck
☐	5444394	August 1995	Watson et al.
☐	5448186	September 1995	Kawata
☐	5455525	October 1995	Ho et al.

☐	5457644	October 1995	McCollum	
☐	5465375	November 1995	Thepaut et al.	
☐	5473266	December 1995	Ahanin et al.	
☐	5473267	December 1995	Stansfield	
☐	5475583	December 1995	Bock et al.	
☐	5475803	December 1995	Stearns et al.	
☐	5475856	December 1995	Kogge	
☐	5483620	January 1996	Pechanek et al.	
☐	5485103	January 1996	Pedersen et al.	
☐	5485104	January 1996	Agrawal et al.	
☐	5489857	February 1996	Agrawal et al.	
☐	5491353	February 1996	Kean	
☐	5493239	February 1996	Zlotnick	
☐	5497498	March 1996	Taylor	
☐	5506998	April 1996	Kato et al.	
☐	5510730	April 1996	El Gamal et al.	
☐	5511173	April 1996	Yamaura et al.	
☐	5513366	April 1996	Agarwal et al.	
☐	5521837	May 1996	Frankle et al.	
☐	5522083	May 1996	Gove et al.	
☐	5532693	July 1996	Winters et al.	
☐	5532957	July 1996	Malhi	
☐	5535406	July 1996	Kolchinsky	
☐	5537057	July 1996	Leong et al.	
☐	5537601	July 1996	Kimura et al.	
☐	5541530	July 1996	Cliff et al.	
☐	5544336	August 1996	Kato et al.	
☐	5548773	August 1996	Kemney et al.	
☐	5555434	September 1996	Carlstedt	
☐	5559450	September 1996	Ngai et al.	
☐	5561738	October 1996	Kinerk et al.	
☐	5570040	October 1996	Lytle et al.	
☐	5574930	November 1996	Halverson, Jr. et al.	395/800
☐	5583450	December 1996	Trimberger et al.	
☐	5586044	December 1996	Agrawal et al.	
☐	5587921	December 1996	Agrawal et al.	
☐	5588152	December 1996	Dapp et al.	
☐	5590345	December 1996	Barker et al.	
☐	5596742	January 1997	Agarwal et al.	
☐	5617547	April 1997	Feeney et al.	

☐	5634131	May 1997	Matter et al.	
☐	5652894	July 1997	Hu et al.	
☐	5655124	August 1997	Lin	
☐	5659797	August 1997	Zandveld et al.	
☐	5713037	January 1998	Wilkinson et al.	
☐	5717943	February 1998	Barker et al.	
☐	5734921	March 1998	Dapp et al.	
☐	5742180	April 1998	Dehon	
☐	5748872	May 1998	Norman	
☐	5754871	May 1998	Wilkinson et al.	
☐	5761484	June 1998	Agarwal et al.	
☐	5778439	July 1998	Timberger et al.	
☐	5794059	August 1998	Barker et al.	
☐	5801715	September 1998	Norman	
☐	5828858	October 1998	Athanas	
☐	5838165	November 1998	Chatter	
☐	5844888	December 1998	Narjjyka	
☐	5867691	February 1999	Shiraishi	
☐	5892961	April 1999	Trimberger et al.	
☐	5915123	June 1999	Mirsky et al.	
☐	5927423	July 1999	Wada et al.	
☐	5936424	August 1999	Young et al.	
☐	5956518	September 1999	DeHon et al.	
☐	6034538	March 2000	Abramovici	
☐	6014509	April 2000	Furtek et al.	
☐	6049222	April 2000	Lawman	326/38
☐	6052773	April 2000	DeHon et al.	
☐	6088795	July 2000	Vorbach et al.	713/100
☐	6054873	August 2000	Laramie	
☐	6108760	September 2000	Mirsky et al.	
☐	6122719	September 2000	Mirsky et al.	
☐	6127908	October 2000	Bozler et al.	
☐	6172520	January 2001	Lawman et al.	326/38
☐	6202182	March 2001	Abramovici et al.	
☐	6282627	August 2001	Wong et al.	

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
4416881.0	November 1994	DE	
19654595	July 1998	DE	

19654846	July 1998	DE
19651075	October 1998	DE
0 221 360	May 1987	EP
19704728	May 1987	EP
0428327	May 1991	EP
748 051	December 1991	EP
0539595	May 1993	EP
0 678 985	October 1995	EP
0707269	April 1996	EP
0 726 532	August 1996	EP
735 685	October 1996	EP
0748051	December 1996	EP
0735685	October 1998	EP
A90/04835	May 1990	WO
WO90/11648	October 1990	WO
A 93/11503	June 1993	WO
94/08399	April 1994	WO
95/00161	January 1995	WO
95/26001	September 1995	WO

OTHER PUBLICATIONS

Villasenor, John, et al., "Configurable Computing." Scientific American, vol. 276, No. 6, Jun. 1997, pp. 66-71.
Villasenor, John, et al., "Configurable Computing Solution for Automatic Target Recognition," IEEE, 1996 pp. 70-79.
Athanas, Peter, et al., "IEEE Symposium on FPGAs For Custom Computing Machines," IEEE Computer Society Press, Apr. 19-21, 1995, pp. i-vii, 1-222.
Bittner, Ray, A., Jr., "Wormhole Run-Time Reconfiguration: Conceptualization and VLSI Design of a High Performance Computing system," Dissertation, Jan. 23, 1997, pp. i-xx, 1-415.
Myers, G., Advances in Computer Architecture, Wiley-Interscience Publication, 2nd ed., John Wiley & Sons, Inc. pp. 463-494, 1978.
M. Saleeba, "A Self-Contained Dynamically Reconfigurable Processor Architecture", Sixteenth Australian Computer Science Conference, ASCS-16, QLD, Australia, Feb., 1993.
M. Morris Mano, "Digital Design," by Prentice Hall, Inc., Englewood Cliffs, New Jersey 07632, 1984, pp. 119-125, 154-161.
Maxfield, C. "Logic that Mutates While-U-Wait" EDN (Bur. Ed) (USA), EDN (European Edition), Nov. 7, 1996, Cahners Publishing, USA.
Norman, Richard S., Hyperchip Business Summary, The Opportunity, Jan. 31, 2000, pp. 1-3.

ART-UNIT: 2182

PRIMARY-EXAMINER: Gaffin; Jeffrey

ASSISTANT-EXAMINER: Mia; Rijue

ATTY-AGENT-FIRM: Kenyon & Kenyon

ABSTRACT:

A method for processing data in a configurable unit having a multidimensional cell arrangement a switching table is provided, the switching table including a controller and a configuration memory. Configuration strings are transmitted from the switching table to a configurable element of the unit to establish a valid configuration. A configurable element writes data into the configuration memory.

The controller of the switching table recognizes individual records as commands and may execute the recognized commands. The controller may also recognize and differentiate between events and execute a action in response thereto. In response to an event, the controller may move the position of a pointer, and if it has received configuration data rather than commands for the controller, sends the configuration data to the configurable element defined in the configuration data. The controller may send a feedback message to the configurable element. The configurable element may recognize and analyze the feedback message. An configurable element may transmit data into the configuration memory of the switching table.

11 Claims, 26 Drawing figures